# Failure Analysis of a Phase Lock Loop Circuit with ESD Strategy Optimization

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**Abstract:** A failure analysis of a Phase lock loop (PLL) due to the ESD structure defects is presented in this paper. ESD is one of the most important reliability issues in the design of integrated circuits. About 40% of the failure of integrated circuits is related to ESD/EOS stress. In order to improve the reliability of ICs, the design of ESD protection is increasingly necessary for the modern semiconductor industry [1, 2]. There are many standards to evaluate the ESD robustness of a circuit, and the HBM and MM model are the most popular criteria. To improve the ESD capability and find out the root of the failure phenomenon, this paper employs some FA tools to deal with the problems, and the optimized solution is given and discussed, which can effectively improve the reliability of the product.

## 1. Introduction

ESD is the most dangerous problem for most ICs, which leads to its failure even perpetual damage because of abnormal electrical stresses. ESD protection circuit is a significant peripheral circuit to ensure the reliability of the integrated circuits, which can avoid them from ESD damage by providing ESD discharging path.

Among the ESD models, HBM is the most common model. As the ESD stress coming from outside and the ESD capability of the circuit is decided by the weakest pins [3], so it is necessary of a whole chip ESD protection design.

This paper selects a typical ESD protection structure failure case, the circuit failure analysis method and optimization design are analyzed. At last, the advices on ESD protection design are given.

## 2. Failure Phenomenon

The failure event is happened to a PLL chip fabricated with a CMOS process, which lose functions after 1kV HBM stress test. Failure chip electric parameters test performance excessive static power supply current shown in table1, and by testing the static impedance between input or output pins and the power or ground, we found the abnormal impedance between three of output

ports and power supply shown in Fig. 1.

The impedances with the order of kΩ are observed, while the qualified circuit exhibits the impedance of MΩ order. In other words, the impedance between three output ports and power supply of failed circuits reduced 1~2 orders compared with qualified circuits.

Table.1. Static power supply current of failure chip

| sample | static power supply current(uA) |
|---|---|
| Qualified product | 1.229 |
| Failed 1# | 227.6 |
| Failed 2# | 244.3 |
| Failed 3# | 239.8 |

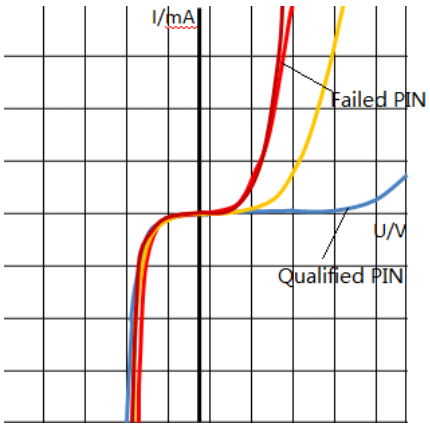


Fig.1. IV curve of failure product

Based on the aforementioned tests, the chip after 1kv HBM ESD test suffered stress damage, which leads to abnormal static impedance between its outputs and power supply, and electric parameter test performance for static power supply current exceeds.

## 3. Failure Location Methodology

Firstly, we examined failure chips using optical microscope, nothing abnormal else founded on the surface. The visual inspection method isn't available for failure location. In the field of failure analysis, Emission Microscope (EMMI) is a versatile tool to locate the failure points. It takes advantage of the electro-luminescent characteristics of silicon devices, providing a photon mapping of the ESD structure during DC measurement without de-layering or destroying the sample. The EMMI experiment image is shown in Fig. 2. The highlight point leaded by the abnormal current of failure output devices is observed at the bottom corner.

To confirm the EMMI experiment results, we performed the following HBM ESD tests: step1, we select qualified products to suffer 1kv HBM static stress with shielding the aforementioned three output ports, and then re-test the electrical parameters after ESD experiments. The experiment results show that the static impedance of stressed ports is all the same with that of the unstressed ones. Step2, we take the 500V HBM ESD test only for the above three output ports and shielding all the other ports, the product failed after 500V HBM ESD test. By further testing, we foundthe static impedance showed abnormal between three output ports and the power supply, which are the same with failed products. Finally we can confirm ESD ability of the three output ports is relatively weaker than all the other ports.

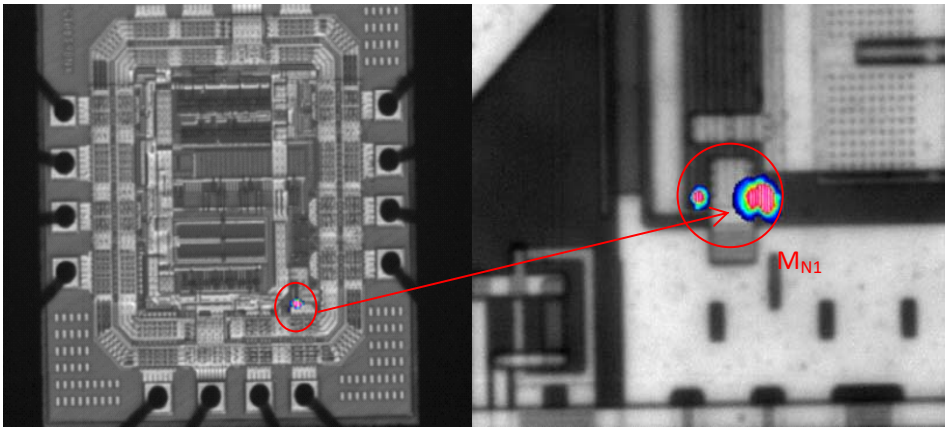


Fig.2. The EMMI experiment image

## 4. Results Analysis and Improvement

According to the product circuit and layout structure, we can estimate that the reason of the above three output ports ESD ability being weak may be the defect of ESD protection circuit structure or chip internal structure. Through the analysis of circuit structure, we found that those three output ports all have ESD protection structure shown in Fig. 3 which are the same with other ports. So we reviewed the chip internal structure and found that there are output devices parallel with each ESD protection circuits shown in Fig. 4.

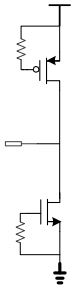

Fig.3. ESD protection structure of failure port.

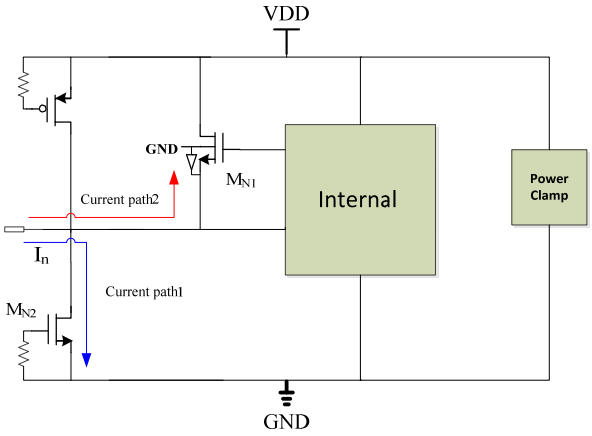


Fig.4. Include internal circuit structure of failure port.

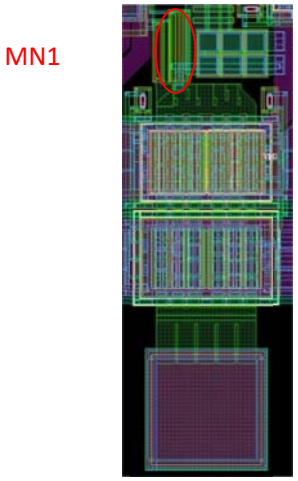


Fig.5. Layout of the failure port.

When the ESD test under the PDmode, In is the positive current to GND. Now there are two current paths in the Fig 4. Actually, MN1 doesn't turn on as a bipolar now since the shunt path to GND including extra power clamp. The path takes higher serial resistance, the harder to conduct the ESD current. The current from the output to GND through MN1 can only be shunted by the parasitic reverse-biased diode of source-body (N+-Psub).For the current path 2, the MN2 conducts the ESD current in bipolar mode to take majority current. However, the breakdown voltage of current path 1 and 2 are determined by the reverse-biased diode of N+ and Psub, leading both the path turn on simultaneously. Generally, the reverse-biased diode sustains very low ESD stress level due to large parasitic resistance. As a result, the current path 1 is prone to be destroyed by ESD stresses comparing with current path2.

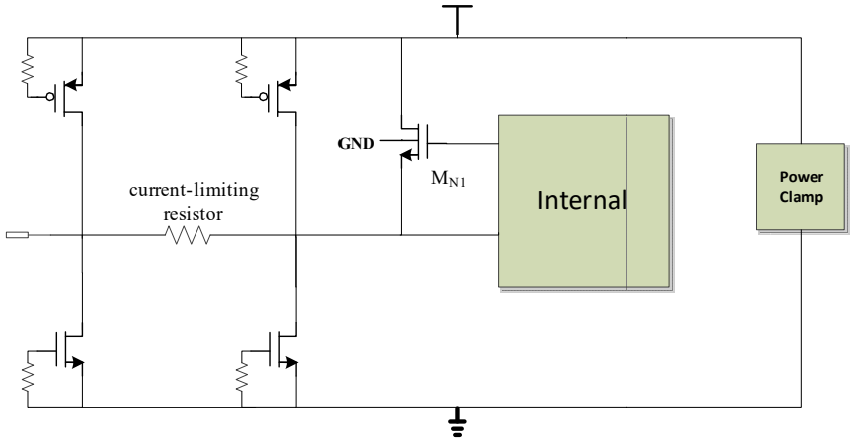


Fig.6. The improved ESD protection structure

Based on the previous analysis, we put forward the following improvement scheme combining with the internal schematic to promote the ESD capability. A current-limiting resistor of 150Ω between the first stage and secondary stage, so the reversed-diode of BE(MN1) will not breakdown to conduct current, protected by the new structure. The improved ESD strategy [4, 5] is shown in Fig. 5 With the Zap master test of HBM model, the modified product can pass the HBM level of 3.5kV. All the analysis procedure and the measurement results prove the effectiveness of the optimized protection method.

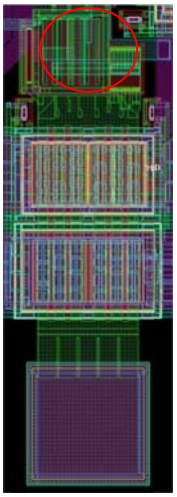


Fig.7. The improved ESD protection Layout

## 5. Conclusions

As the ESD designer understood circuit internal structure insufficiently, the ESD protection strategy maybe not successful at the first time, leading the ESD protection circuit unable to take the expected action when the ESD stresses happen. The reliability and the time to market of the product will be affected.

Through the failure analysis case , we can know that a designer not only need to consider the anti-ESD ability of the protection circuit but also need to consider the internal structure and ESD protection design together, which will affect electrostatic discharge channel and the desired ESD level of product when design the protection structure.

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